

**REMARKS**

In the Office Action under reply, a new title was required. By this Response, an appropriate title is submitted.

In addition, the Examiner required the legend "Prior Art" be added to Fig. 1. However, this legend was added to Fig. 1 when the instant application was filed. A copy of the replacement sheet that accompanied the filing of this application is enclosed.

In the Office Action, claims 5-10, all the claims present in this application, were rejected under 35 USC 112, first paragraph, as allegedly defining subject matter that is not supported by Applicants' disclosure. Reconsideration and withdrawal of this rejection is respectfully requested for the following reasons.

The Examiner contends that the following recitations in claim 5 find no support in Applicants' specification:

"a delay section comprising a series of buffer memories that are serially connected for storing N pixels of image data, the delay section receiving input of image data read out by the readout section to one end of the series of buffer memories and outputting delayed image data from each of the buffer memories; and

a section for conducting signal processing of image data in the horizontal or vertical direction by weighting and compositing the image data outputted from each of the buffer memories."

The Examiner's attention is directed to the following portions of Applicants' published application, which fully support the aforequoted recitations of claim 1.

Paragraph [0080] describes resolution conversion circuit 28, shown in Fig. 7, which includes horizontal correction buffer 72, transform processing circuit 73, vertical direction buffer 74 and transform processing circuit 25. Paragraph [0085] points out that transform processing circuit 73 weights the image data in "in a pre-set fashion with pre-set weights and synthesizes the

weighted image data...". Paragraph [0086] points out that vertical direction buffer 74 "is constituted by a serial connection of first to third buffers 91, 92, 93, each adapted to produce a one-line delay." Paragraph [0089] points out that transform processing circuit 75 weights the image data "in a pre-set fashion with pre-set weights and synthesizes the weighted image data...". Accordingly, vertical direction buffer 74 corresponds to the "delay section" recited in claim 5; and transform processing circuit 75 corresponds to the "section for conducting signal processing" also recited in claim 5.

In addition, memory controller 22 reads out a page of image data from image memory 32 (paragraph [0092]) by reading out N pixels on a line basis in the horizontal correction in row-by-row sequence (paragraph [0093]). Image data of N pixels offset by one line is stored in each of buffer memories 91, 92 and 93 (paragraph [0097]). As pointed out in paragraph [0100], conversion circuit 28, such as shown in Fig. 7, can be used for resolution conversion in the vertical or horizontal directions. See also paragraphs [0101] and [0102].

The output from resolution conversion circuit 28 is supplied to encoder 23, which has a simplified resolution conversion circuit 23a that is similar to conversion circuit 28 (paragraph [0103]). Resolution conversion circuit 23a is shown in Fig. 15 as including a line memory 101 that supplies a line of image data to interpolation circuit 102 that weights the image data "with a pre-set weighting to perform linear interpolation in the vertical direction" (paragraph [0106]).

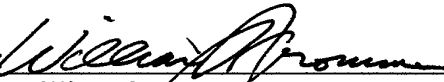
It is clear from the foregoing explanation and reference to Applicants' specification and drawings that the recitations in claim 5, particularly noted by the Examiner, find full and complete support in Applicants' disclosure. Therefore, all of the recitations in claim 5 are properly disclosed in accordance with 35 USC 112, first paragraph. Consequently, the withdrawal of the rejection of this claim is respectfully requested.

The Examiner rejected independent claim 9 for the same reason used to reject claim 5. It is assumed, however, since claim 9 depends from claim 8 and since claim 8 is directed to the method performed by the imaging apparatus defined by claim 5, the Examiner intended to reject claim 8 for the same reason used to reject claim 5. The explanation set out above demonstrates where in Applicants' disclosure there is full support for the recitations of claim 8. Accordingly, the withdrawal of the rejection of claim 8 is respectfully requested.

Applicants' disclosure describes the subject matter defined by claims 5-10 in compliance with the requirements of 35 USC 112, first paragraph. Consequently, the rejection of these claims should be withdrawn. As a result, claims 5-10 are in condition for allowance; and early notice to this effect is respectfully requested.

Respectfully submitted,

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